



ALPHA DATA

ADM-VPX3-9Z5

User Manual

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Table Of Contents

| | | |
|----------|--|----------|
| 1 | Introduction | 1 |
| 1.1 | Key Features | 1 |
| 1.2 | References & Specifications | 1 |
| 1.3 | Order Code | 1 |
| 2 | Installation | 3 |
| 2.1 | Handling Instructions | 3 |
| 2.2 | Hardware Installation | 3 |
| 2.2.1 | System Requirements | 3 |
| 2.2.2 | Cooling Requirements | 3 |
| 2.3 | Software Installation | 4 |
| 3 | Functional Description | 5 |
| 3.1 | Overview | 5 |
| 3.1.1 | Switch Definitions | 6 |
| 3.1.2 | LED Definitions | 7 |
| 3.2 | VPX P0 Interface | 9 |
| 3.2.1 | SYSRESET# | 9 |
| 3.2.2 | AUXCLK | 9 |
| 3.2.3 | REFCLK | 9 |
| 3.3 | VPX P1 GPIO | 9 |
| 3.3.1 | Differential / Low Voltage GPIO | 9 |
| 3.3.2 | Single Ended PSMIO GPIO | 9 |
| 3.4 | VPX P2 GPIO | 10 |
| 3.4.1 | Differential / Low Voltage GPIO | 10 |
| 3.4.2 | Single Ended GPIO | 10 |
| 3.5 | JTAG Interface | 11 |
| 3.5.1 | On-board Interface | 11 |
| 3.5.2 | VPX Interface | 11 |
| 3.5.3 | JTAG Voltages | 11 |
| 3.6 | Clocks | 12 |
| 3.6.1 | IO Delay Reference Clock (FABRIC_CLK) | 13 |
| 3.6.2 | IO Delay Reference Clock (MEM_CLK) | 13 |
| 3.6.3 | Fixed 100MHz Reference clock REFCLK100M | 13 |
| 3.6.4 | Selectable Clocks (CLKA and CLKB) | 13 |
| 3.6.5 | Module to Carrier Global Clocks (CLK_M2C) | 14 |
| 3.6.6 | Module to Carrier MGTREF Clocks (GBTCLK_M2C) | 14 |
| 3.6.7 | PS_REFCLK | 14 |
| 3.7 | Resets | 15 |
| 3.8 | Zynq PS Block | 15 |
| 3.8.1 | Boot Modes | 15 |
| 3.8.2 | PS Memory Interfaces | 15 |
| 3.8.2.1 | Quad SPI Flash Memory | 15 |
| 3.8.2.2 | MicroSD Card | 15 |
| 3.8.2.3 | PS DDR4 Memory | 15 |
| 3.8.3 | PS MIO | 15 |
| 3.8.4 | PS MGT Links | 16 |
| 3.9 | Zynq PL Block | 16 |
| 3.9.1 | I/O Bank Voltages | 16 |
| 3.9.2 | PL MGT Links | 16 |
| 3.9.3 | FMC+ GPIO Interface | 17 |
| 3.9.4 | VPX P1 GPIO Interface | 17 |
| 3.9.5 | VPX P2 GPIO Interface | 17 |
| 3.9.6 | PL DDR4 Memory | 18 |

| | | |
|-------------------|---|-----------|
| 3.10 | System Monitoring | 18 |
| 3.10.1 | Automatic Temperature Monitoring | 18 |
| 3.10.2 | System Monitor Status LEDs | 19 |
| 3.11 | FMC Interface and Front-Panel I/O | 19 |
| Appendix A | P1 Pin Assignments | 21 |
| A.1 | Data Plane 1 (P1 Wafers 1-4) | 21 |
| A.2 | Data Plane 2 (P1 Wafers 5-8) | 21 |
| A.3 | User Plane PS GTR(P1 Wafers 9-10) | 22 |
| A.4 | User Plane GPIO(P1 Wafers 11-12) | 22 |
| A.5 | User Plane PS MIO(P1 Wafers 9-14) | 22 |
| A.6 | Control Plane (P1 Wafers 15-16) | 22 |
| Appendix B | P2 Pin Assignments | 23 |
| B.1 | GPIO (P2 Wafers 1-4) | 23 |
| B.2 | MGT Pins (P2 Wafers 5-16) | 23 |
| Appendix C | FMC Pin Assignments | 25 |
| C.1 | GPIO Pins | 25 |
| C.2 | Clock Pins | 27 |
| C.3 | MGT Pins | 28 |

List of Tables

| | | |
|----------|---|----|
| Table 1 | References | 1 |
| Table 2 | Build Options | 2 |
| Table 3 | Processor Setup Switch Definitions (SW1) | 6 |
| Table 4 | VPX Control Switch Definitions (SW2) | 6 |
| Table 5 | Status LED Definitions | 8 |
| Table 6 | User Defined LEDs | 8 |
| Table 7 | FABRIC_CLK Connections | 13 |
| Table 8 | MEM_CLK Connections | 13 |
| Table 9 | REFCLK100M Connections | 13 |
| Table 10 | CLKA Connections | 13 |
| Table 11 | CLKB Connections | 14 |
| Table 12 | CLK_M2C Connections | 14 |
| Table 13 | GCLK_M2C Connections | 14 |
| Table 14 | PS_REFCLK Connection | 15 |
| Table 15 | Reset Switches | 15 |
| Table 16 | Boot Mode Selection | 15 |
| Table 17 | VPX PS MIO Groups | 16 |
| Table 18 | PS MGT Links | 16 |
| Table 19 | PL FPGA IO Banks | 16 |
| Table 20 | PL MGT Links | 16 |
| Table 21 | FMC+ Groups (J1) | 17 |
| Table 22 | VPX P1 GPIO Groups | 17 |
| Table 23 | VPX P2 GPIO Groups | 18 |
| Table 24 | Voltage and Temperature Monitors (in microcontroller) | 18 |
| Table 25 | Temperature Limits | 19 |
| Table 26 | System Monitor Status LEDs | 19 |
| Table 27 | Data Plane 1 (P1 Wafers 1-4) | 21 |
| Table 28 | Data Plane 2 (P1 Wafers 5-8) | 21 |
| Table 29 | User Plane PS GTR(P1 Wafers 9-10) | 22 |
| Table 30 | User Plane GPIO(P1 Wafers 11-12) | 22 |

| | | |
|----------|---|----|
| Table 31 | User Plane PS MIO(P1 Wafers 9-14) | 22 |
| Table 32 | Control Plane (P1 Wafers 15-16) | 22 |
| Table 33 | GPIO (P2 Wafers 1-4) | 23 |
| Table 34 | MGT (P2 Wafers 5-16) | 23 |
| Table 35 | GPIO Pins | 25 |
| Table 36 | Clock Pins | 27 |
| Table 37 | MGT Pins | 28 |

List of Figures

| | | |
|----------|----------------------------------|----|
| Figure 1 | ADM-VPX3-9Z5 | 4 |
| Figure 2 | ADM-VPX3-9Z5 Block Diagram | 5 |
| Figure 3 | LED Locations | 7 |
| Figure 4 | JTAG Boundary Scan Chain | 11 |
| Figure 5 | Clocks | 12 |

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1 Introduction

The **ADM-VPX3-9Z5** is a high performance Defense Grade reconfigurable 3U OpenVPX format board based on the Xilinx Zynq Ultrascale+ range of Multiprocessor System-on-Chips (MPSoC).

1.1 Key Features

Key Features

- 3U Open VPX, compliant to VITA Standards 46.0 and 65
- All parts shall be Defense Grade -55 to +125 Deg C (or commercial pin compatible equivalent)
- FMC+ interface compliant to Vita 57.4 with high density connector
- Support for Zynq Ultrascale+ ZU19EG and ZU11EG MPSoC in the C1760 (42.5 x 42.5) package
- Support for Xilinx low-voltage (LVAUX) operation
- VPX P1 and P2 utilized according to OpenVPX payload slot profile SLT3-PAY-2F2U-14.2.3
- Processing System (PS) Block consisting of:
 - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
 - 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC
 - Removable microSD Flash memory (/DEV variant only)
 - Two Quad SPI Flash memory, up to 2Gb each
- Programmable Logic (PL) block consisting of:
 - 653k logic cells (ZU11EG) or 1143k logic cells (ZU19EG)
 - 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC
- 4-lanes of HSSIO on the PS block which connect to the control plane and the user defined area on P1.
- Voltage and temperature monitoring
- Air-cooled and conduction-cooled configurations

1.2 References & Specifications

| | |
|-----------------|--|
| ANSI/VITA 46.0 | <i>VPX Baseline Standard, October 2007, VITA, ISBN 1-885731-44-2</i> |
| ANSI/VITA 46.4 | <i>PCI Express® on the VPX Fabric Connector, July 2010, VITA, Draft 0.15</i> |
| ANSI/VITA 46.6 | <i>Gigabit Ethernet Control Plane on VPX, September 2010, VITA, Draft 0.7</i> |
| ANSI/VITA 46.9 | <i>PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard, November 2010, VITA, ISBN 1-885731-63-9</i> |
| ANSI/VITA 46.11 | <i>System Management on VPX, June 2015, VITA, ISBN 1-885731-84-1</i> |
| ANSI/VITA 48.2 | <i>Mechanical Specifications for Microcomputers Using REDI Conduction Cooling Applied to VITA VPX, July 2010, VITA, ISBN 1-885731-60-4</i> |
| ANSI/VITA 57.1 | <i>FPGA Mezzanine Card (FMC) Standard, July 2008, VITA, ISBN 1-885731-49-3</i> |
| ANSI/VITA 65 | <i>OpenVPX™ System Specification, June 2010, VITA, ISBN 1-885731-58-2</i> |
| ANSI/VITA 57.4 | <i>FPGA Mezzanine Card Plus(FMC+) Standard, March 2016, VITA, Draft</i> |

Table 1 : References

1.3 Order Code

ADM-VPX3-9Z5/z-2(c)

| Name | Symbol | Configurations |
|---------------|--------|--|
| Configuration | T | /CC4/PB = XQZU19EG-1M Q Grade FPGA / Cond. Cooled MIL temp / Sn-Pb Solder /Z19-2/CC3/PB = XQZU19EG-2I Q Grade FPGA / Cond. Cooled IND temp / Sn-Pb Solder |

Table 2 : Build Options

Not all combinations may be available. Please check with Alpha Data sales for details.

2 Installation

2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:



- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 Hardware Installation

2.2.1 System Requirements

The ADM-VPX3-9Z5 is a 3U OpenVPX compliant FPGA card with FMC front IO interface.

Alpha Data offers a Rear Transition Module (RTM) that breaks out all P2 IO and P1 control lanes (Part number: ADM-VPX3-9Z5-RTM).

2.2.2 Cooling Requirements

The power dissipation of the board is highly dependent on the FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the approximate current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heatsink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and appropriate metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See [Section System Monitoring](#) for health monitoring details.

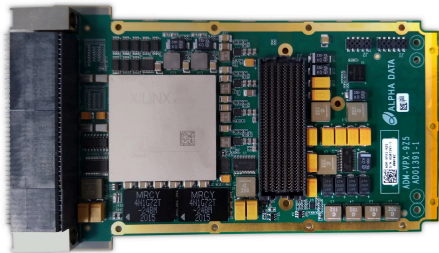


Figure 1 : ADM-VPX3-9Z5

2.3 Software Installation

Please refer to the Reference Designs on the Alpha Data Download Site. Example projects for configuring the Zynq UltraScale+ MPSOC device and example software for running on the ARM CPUs can be downloaded from there.

3 Functional Description

3.1 Overview

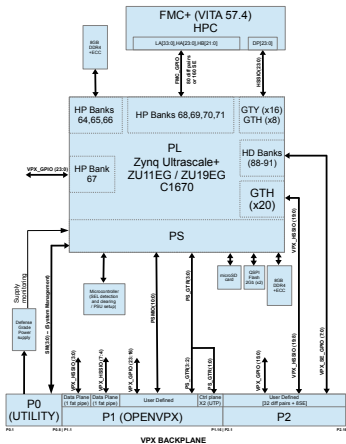


Figure 2 : ADM-VPX3-9Z5 Block Diagram

3.1.1 Switch Definitions

There are two sets of eight DIP switches placed on the bottom of the board. Their functions are described below.

Note:

All switches are OFF by default. Factory Configuration switch must be in the OFF position for normal operation.

| Switch Ref. | Function | ON State | Off State |
|-------------|----------------|---|--------------------------|
| SW1-(4:1) | PS_MODE(3:0) | PS Boot Mode - see section Boot Modes | |
| SW1-5 | Hardware Reset | Hardware Reset (complete restart) | Normal Operation |
| SW1-6 | Software Reset | Software Reset (warm reset) | Normal Operation |
| SW1-7 | PS_SE_EN | PS Single Ended enabled | PS Single Ended disabled |
| SW1-8 | P2_SE_EN | P2 Single Ended enabled | P2 Single Ended disabled |

Table 3 : Processor Setup Switch Definitions (SW1)

| Switch Ref. | Function | ON State | Off State |
|-------------|-----------------------|-----------------------------|------------------------------|
| SW2-1 | P1_LVDS_EN | P1 low voltage GPIO Enabled | P1 low voltage GPIO Disabled |
| SW2-2 | CLKA_SEL | CLKA = 100MHz | CLKA = 125MHz |
| SW2-3 | CLKB_SEL | CLKB = 161.13MHz | CLKB = 156.25MHz |
| SW2-4 | User Switch | PSMIO26=logic low | PSMIO26=logic high |
| SW2-5 | VPX JTAG | Connect JTAG chain to P0 | Isolate JTAG chain from P0 |
| SW2-6 | P2_LVDS_EN | P2 low voltage GPIO Enabled | P2 low voltage GPIO Disabled |
| SW2-7 | Factory Configuration | - | Normal Operation |
| SW2-8 | LVAUX_EN | LVAUX mode enabled | Normal Operation |

Table 4 : VPX Control Switch Definitions (SW2)

3.1.2 LED Definitions

There are seven LEDs to provide a visual indication of the board status.

Their locations are shown in [Figure 3](#)

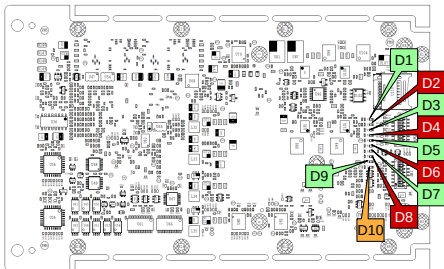


Figure 3 : LED Locations

| Comp. Ref. | Function | ON State | Off State |
|-------------|-----------------------|--------------------------------|------------------------------------|
| D3 (Green) | System Monitor Status | See Table 26 | |
| D6 (Red) | System Monitor Status | See Table 26 | |
| D9 (Green) | FPGA (PL) Done | PL is configured | PL is not configured |
| D10 (Amber) | VPX JTAG STATUS | JTAG chain Connected to VPX P0 | JTAG chain isolated from VPX P0 |
| D2 (Red) | Power Fault | Power Supply Fault | Power Supplies off or within range |
| D8 (Red) | PS Error | PS Error | Normal Operation |
| D7 (Green) | PS Status | Normal Operation | PS is in Reset / Error |

Table 5 : Status LED Definitions

There also are three user defined LEDs available:

| Comp. Ref. | FPGA Pin | Bank | Operation |
|------------|----------|------------|--------------------|
| D4 (Red) | D9 | PL Bank 93 | Logic low = LED ON |
| D5 (Green) | C9 | PL Bank 93 | Logic low = LED ON |
| D1 (Green) | U28 | PSMIO 46 | Logic low = LED ON |

Table 6 : User Defined LEDs

3.2 VPX P0 Interface

3.2.1 SYSRESET#

When the 9Z5 is NOT acting as the system controller:

- SYSRESET# is an active low input from the system controller
- SYSRESET# is connected to the FPGA PL side PERSTN0 PCIe reset pin on Bank 65 (Pin AM25)
- SYSRESET# is connected to the FPGA PS side PS_POR_B hard reset pin on Bank 503 (Pin W27)

When the 9Z5 is acting as the system controller:

- SYSRESET# is an active low output to the rest of the system
- SYSRESET# is driven from PSMIO 56 (Pin AA30)

3.2.2 AUXCLK

Auxiliary Clock. In OpenVPX this clock line can be used for 1PPS synchronization signaling and is an INPUT to the FPGA at Bank93 pin G8 (LVCMOS33) .

3.2.3 REFCLK

Reference Clock. This clock is an input to the onboard clock distribution and generation system. In OpenVPX this 50MHz clock can be used to align all system clocks.

When the 9Z5 is NOT acting as a system controller this clock is an INPUT to the FPGA at Bank93 pin F8 (LVCMOS33)

When the 9Z5 IS acting as a system controller this clock is an OUTPUT from the FPGA at Bank93 pin G7 (LVCMOS33)

3.3 VPX P1 GPIO

3.3.1 Differential / Low Voltage GPIO

In normal operating mode these differential GPIO on P1 are compatible with 1.8V signaling such as LVDS and 1.8V single ended signals.

In LVAUX operating mode the GPIO on P1 are compatible with 1.2V signaling such as LVDS_12 and 1.2V single ended signals.

These signals are routed differentially to/from FPGA Bank 67 and are enabled / disabled via switch SW2-1.

The FPGA can NOT accept signal levels above 1.8V (normal operation) or above 1.2V (LVAUX mode) on these signals, **otherwise damage to the FPGA device may occur.**

 Care must be taken to ensure that the acceptable signal limits will not be exceeded prior to enabling these GPIO lines.

3.3.2 Single Ended PSMIO GPIO

The Single Ended GPIO on P1 are compatible with 3.3V single ended signals and are routed from PSMIO on Bank 501.

The FPGA is protected from inappropriate signal levels by a low resistance quick switch and can accept up to 3.3V on an input.

These signals are are enabled / disabled via switch SW1-7.

3.4 VPX P2 GPIO

3.4.1 Differential / Low Voltage GPIO

In normal operating mode the differential GPIO on P2 are compatible with 1.8V signaling such as LVDS and 1.8V single ended signals.

In LVAUX operating mode the GPIO on P2 are compatible with 1.2V signaling such as LVDS_12 and 1.2V single ended signals.

These signals are routed differentially to/from FPGA Bank 67 and are enabled / disabled via switch SW2-6.

The FPGA can NOT accept signal levels above 1.8V (normal operation) or above 1.2V (LVAUX mode) on these signals, **otherwise damage to the FPGA device may occur.**



Care must be taken to ensure that the acceptable signal limits will not be exceeded prior to enabling these GPIO lines.

3.4.2 Single Ended GPIO

The Single Ended GPIO on P2 are routed to/from FPGA bank 94 and are compatible with 3.3V single ended signals.

The FPGA is protected from inappropriate signal levels by a low resistance quick switch and can accept up to 3.3V on an input.

These signals are enabled / disabled via switch SW1-8.

3.5 JTAG Interface

3.5.1 On-board Interface

A JTAG boundary scan chain is connected to header J1. This allows the connection of the Xilinx JTAG cable via adapter board AD-JTAG-ADPT2.

Adapter board AD-JTAG-ADPT2 should be inserted into header J1 through the rear of the board, header J1 is keyed to ensure correct orientation.

The scan chain is shown in [Figure JTAG Boundary Scan Chain](#):

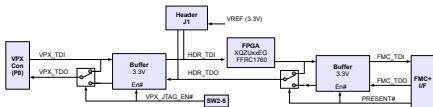


Figure 4 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the VPX backplane (SW2-5 is ON), header J1 should not be used.

3.5.2 VPX Interface

The JTAG interface on the VPX backplane is normally unused. When SW2-5 is OFF (default), all JTAG signals to P0 are left floating.

The JTAG interface can be connected to the VPX Backplane (through level-translators) by switching SW2-5 ON.

3.5.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on J1 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the VPX interface use 3.3V signal levels and are connected through buffers to the on-board scan chain.

The JTAG signals at the FMC interface also use 3.3V signal levels and are connected through buffers to FMC boards scan chain.

3.6 Clocks

The **ADM-VPX3-9Z5** board provides a wide variety of clocking options. In addition to the clocks routed from the FMC+ connector, the board has 4 selectable fixed frequency clock sources. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

A complete overview of the clock routing on the **ADM-VPX3-9Z5** is given in [Clocks](#). A description of each clock follows.

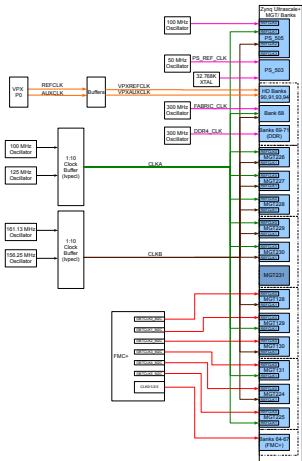


Figure 5 : Clocks

3.6.1 IO Delay Reference Clock (FABRIC_CLK)

The fixed reference clock FABRIC_CLK is a differential LVDS signal.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|------------|-----------|-------------------|-------------|---------|---------|
| FABRIC_CLK | 300 MHz | IO BANK 67 | LVDS | AT13 | AT12 |

Table 7 : FABRIC_CLK Connections

3.6.2 IO Delay Reference Clock (MEM_CLK)

The fixed reference clock MEM_CLK is a differential LVDS signal.

MEM_CLK is used as the reference clock for the PL DDR memory logic.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---------|-----------|-------------------|-------------|---------|---------|
| MEM_CLK | 300 MHz | IO BANK 67 | LVDS | AT11 | AT10 |

Table 8 : MEM_CLK Connections

3.6.3 Fixed 100MHz Reference clock REFCLK100M

A fixed 100MHz reference clock is available on the board.

| Signal | Frequency | Target FPGA Input | IO Standard | "P" pin |
|------------|-----------|--------------------|-------------|---------|
| REFCLK100M | 100 MHz | PS_505_MGTREFCLK_0 | LVDS | AG37 |

Table 9 : REFCLK100M Connections

3.6.4 Selectable Clocks (CLKA and CLKB)

There are two selectable clock sources that are forwarded throughout the FPGA. CLKA can be set to either 100MHz or 125MHz. CLKB can be set to either 161.13MHz or 156.25MHz.

| Signal | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---------|--------------------|-------------|---------|---------|
| CLKA[0] | PS_505_MGTREFCLK_1 | LVPECL | AE37 | AE38 |
| CLKA[1] | Bank 67 | LVDS | AP10 | AR10 |
| CLKA[2] | MGTREFCLK_224 | LVPECL | AK12 | AK11 |
| CLKA[3] | MGTREFCLK_225 | LVPECL | AH12 | AH11 |
| CLKA[4] | MGTREFCLK_226 | LVPECL | AF12 | AF11 |
| CLKA[5] | MGTREFCLK_227 | LVPECL | AD12 | AD11 |
| CLKA[6] | MGTREFCLK_228 | LVPECL | AB12 | AB11 |
| CLKA[7] | MGTREFCLK_129 | LVPECL | U32 | U33 |
| CLKA[8] | MGTREFCLK_131 | LVPECL | J32 | J33 |
| CLKA[9] | MGTREFCLK_230 | LVPECL | U10 | U9 |

Table 10 : CLKA Connections

Note: CLKA[9:0] are all buffered copies of the same clock signal.

| Signal | Target FPGA Input | IO Standard | "P" pin | "N" pin |
|---------|--------------------|-------------|---------|---------|
| CLKB[0] | PS_505_MGTREFCLK_2 | LVPECL | AC37 | AC38 |
| CLKB[1] | Bank 67 | LVDS | AR13 | AR12 |
| CLKB[2] | MGTREFCLK_224 | LVPECL | AJ10 | AJ9 |
| CLKB[3] | MGTREFCLK_225 | LVPECL | AG10 | AG9 |
| CLKB[4] | MGTREFCLK_226 | LVPECL | AE10 | AE9 |
| CLKB[5] | MGTREFCLK_227 | LVPECL | AC10 | AC9 |
| CLKB[6] | MGTREFCLK_228 | LVPECL | AA10 | AA9 |
| CLKB[7] | MGTREFCLK_128 | LVPECL | AA32 | AA33 |
| CLKB[8] | MGTREFCLK_130 | LVPECL | N32 | N33 |
| CLKB[9] | MGTREFCLK_229 | LVPECL | W10 | W9 |

Table 11 : CLKB Connections

Note: CLKB[9:0] are all buffered copies of the same clock signal.

3.6.5 Module to Carrier Global Clocks (CLK_M2C)

A connected FMC+ board can generate a number of differential Global clocks (as per the FMC standard). They each connect to a global clock input on the FPGA.

| Signal | Frequency | FPGA Input | IO Standard | "P" pin | "N" pin |
|-----------|-----------|------------|-------------|---------|---------|
| CLK_M2C_0 | Variable | Bank 71 | LVDS | F23 | F22 |
| CLK_M2C_1 | Variable | Bank 71 | LVDS | G22 | G21 |
| CLK_M2C_2 | Variable | Bank 70 | LVDS | H25 | H26 |
| CLK_M2C_3 | Variable | Bank 70 | LVDS | H24 | G25 |

Table 12 : CLK_M2C Connections

3.6.6 Module to Carrier MGTREF Clocks (GBTCLK_M2C)

A connected FMC board can generate a number of differential MGT Reference clocks (as per the FMC standard). They each connect to an MGTREFCLK input on the FPGA.

| Signal | Frequency | FPGA Input | IO Standard | "P" pin | "N" pin |
|--------------|-----------|---------------|-------------|---------|---------|
| GBTCLK_0_M2C | Variable | MGTREFCLK_128 | LVDS | AB34 | AB35 |
| GBTCLK_1_M2C | Variable | MGTREFCLK_129 | LVDS | W32 | W33 |
| GBTCLK_2_M2C | Variable | MGTREFCLK_130 | LVDS | R32 | R33 |
| GBTCLK_3_M2C | Variable | MGTREFCLK_131 | LVDS | L32 | L33 |
| GBTCLK_4_M2C | Variable | MGTREFCLK_229 | LVDS | Y12 | Y11 |
| GBTCLK_5_M2C | Variable | MGTREFCLK_230 | LVDS | V12 | V11 |

Table 13 : GCLK_M2C Connections

3.6.7 PS_REFCLK

The PS reference clock is an independent 50.0MHz reference clock. This is the master clock of the PS side of the MPSoC.

| Signal | Frequency | FPGA Input | IO Standard | pin |
|-----------|-----------|-----------------------|-------------|------|
| PS_REFCLK | 50MHz | PS_REF_CLK (Bank 503) | LVCOS33 | AC27 |

Table 14 : PS_REFCLK Connection

3.7 Resets

The Zynq PS can be reset via two switches, SW1-5 and SW1-6.

| Switch | Reset Type | Effect |
|--------|-------------------------------|--|
| SW1-5 | Power on Reset (PS_POR_B pin) | Clears all logic. Mode pins sampled (i.e. reconfigures hardware). Reboots MPSoC. |
| SW1-6 | Soft Reset (PS_SRST_B pin) | Same as Power on Reset - but does not sample Mode pins (hardware configuration unchanged). |

Table 15 : Reset Switches

3.8 Zynq PS Block

3.8.1 Boot Modes

| PS_MODE3 (SW1-4) | PS_MODE2 (SW1-3) | PS_MODE1 (SW1-2) | PS_MODE0 (SW1-1) | Boot Mode |
|------------------|------------------|------------------|------------------|------------------------------|
| ON | ON | ON | ON | JTAG |
| ON | ON | ON | OFF | Quad SPI (24 bit addressing) |
| ON | ON | OFF | ON | Quad SPI (32 bit addressing) |
| ON | ON | OFF | OFF | SD Flash - SD 2.0 |

Table 16 : Boot Mode Selection

Note: all other possible switch settings are reserved / invalid.

3.8.2 PS Memory Interfaces

The memory devices attached to the PS side of the MPSoC are outlined below.

3.8.2.1 Quad SPI Flash Memory

The ADM-VPX3-9Z5 has two Quad SPI Flash devices, up to 512Mb each. They can be interfaced separately in x1,x2,x4 modes or together in x8 mode.

3.8.2.2 MicroSD Card

The ADM-VPX3-9Z5 can interface to a MicroSD card (SD 2.0 standard at 3.3V).

The uSD card should be fitted in socket U110.

3.8.2.3 PS DDR4 Memory

The PS side of the MPSoC is connected to 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC

3.8.3 PS MIO

11 PS MIO pins are available on VPX connector P1, which can be used to connect internal PS peripherals

through to an RTM module.

| Group | FPGA Bank | Name | Function |
|--------|-----------|-------------|-----------------|
| GPIO_3 | PS501 | PSMIO(10:0) | 11 single-ended |

Table 17 : VPX PS MIO Groups

3.8.4 PS MGT Links

There are a total of 4 Multi-Gigabit Transceiver (MGT) links connected to the PS side of the FPGA:

| Links | Banks | Width | Max Rate | Connection |
|--------------|-------|-------|----------|--|
| PS_GTR (1:0) | 505 | 2 | 6Gbps | GTR links to VPX P1 Connector Ctrl planes (2 ultra thin pipes) |
| PS_GTR (3:2) | 505 | 2 | 6Gbps | GTR links to VPX P1 Connector user defined area |

Table 18 : PS MGT Links

3.9 Zynq PL Block

3.9.1 I/O Bank Voltages

The FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in [PL FPGA IO Banks](#).

| IO Banks | Voltage | Purpose |
|------------|--------------|--------------------------|
| 68, 70, 71 | FMC_VADJ | FMC+ GPIO - LA and HA |
| 69 | FMC_VIO_B | FMC+ GPIO - HB |
| 48 | 1.8V or 1.2V | VPX P2 Differential GPIO |
| 64, 65, 66 | 1.2V | PL DDR4 Banks |
| 94 | 3.3V | VPX P2 Single Ended GPIO |
| 93 | 3.3V | Setup and Control |
| 90, 91 | 3.3V | Unused |

Table 19 : PL FPGA IO Banks

3.9.2 PL MGT Links

There are a total of 48 Multi-Gigabit Transceiver (MGT) links connected to the FPGA, 4 of which are unused. These are connected as follows:

| Links | Banks | Width | Max Rate | Connection |
|----------------|--------------------|-------|----------|--|
| HSSIO(15:0) | 128, 129, 130, 131 | 16 | 28Gbps | GTU links to FMC+ Socket (J3) |
| HSSIO(23:16) | 229, 230 | 8 | 16Gbps | GTH links to FMC+ Socket (J3) |
| VPX_HSSIO(7:0) | 224, 225 | 8 | 16Gbps | VPX P1 Connector Data Planes (2 fat pipes) |

Table 20 : PL MGT Links (continued on next page)

| Links | Banks | Width | Max Rate | Connection |
|-----------------|----------|-------|----------|------------------------------------|
| VPX_HSSIO(19:8) | 224, 225 | 12 | 16Gbps | VPX P2 Connector User Defined Area |
| UNUSED(3:0) | 231 | 4 | - | unused - not routed out |

Table 20 : PL MGT Links

3.9.3 FMC+ GPIO Interface

The FMC+ Connector (J3) has GPIO connections arranged as follows:

| Group | FPGA Bank | Name | Function |
|-------|-----------|---------------|--|
| LA_0 | 71 | LA(16:2) | 14 diff. Pairs / 28 single-ended |
| | | LA_CC (1:0) | 2x Regional Clocks / GPIO pairs / 4 single-ended |
| LA_1 | 70 | LA(33:19) | 15 diff. Pairs / 30 single-ended |
| | | LA_CC (18:17) | 2x Regional Clocks / GPIO pairs / 4 single-ended |
| HA_0 | 68 | HA(16:2) | 15 diff. Pairs / 30 single-ended |
| | | HA_CC (1:0) | 2x Regional Clocks / GPIO pairs / 4 single-ended |
| | | HA(23:18) | 6 diff. Pairs / 12 single-ended |
| | | HA_CC (17) | Regional Clock / GPIO pair / 2 single-ended |
| HB_0 | 69 | HB(5:1) | 5 diff. Pairs / 10 single-ended |
| | | HB(16:7) | 10 diff. Pairs / 20 single-ended |
| | | HB(21:18) | 4 diff. Pairs / 8 single-ended |
| | | HB_CC (0) | Regional Clock / GPIO pair / 2 single-ended |
| | | HB_CC (6) | Regional Clock / GPIO pair / 2 single-ended |
| | | HB_CC (17) | Regional Clock / GPIO pair / 2 single-ended |

Table 21 : FMC+ Groups (J1)

3.9.4 VPX P1 GPIO Interface

The P1 VPX Connector has GPIO connections arranged as follows:

| Group | FPGA Bank | Name | Function |
|--------|-----------|-----------------|--------------------------------|
| GPIO_1 | 67 | VPX_GPIO(23:16) | 4 diff. Pairs / 8 single-ended |

Table 22 : VPX P1 GPIO Groups

3.9.5 VPX P2 GPIO Interface

The P2 VPX Connector has GPIO connections arranged as follows:

| Group | FPGA Bank | Name | Function |
|--------|-----------|------------------|---------------------------------|
| GPIO_0 | 67 | VPX_GPIO(15:0) | 8 diff. Pairs / 16 single-ended |
| GPIO_2 | 94 | VPX_SE_GPIO(7:0) | 8 single-ended |

Table 23 : VPX P2 GPIO Groups

3.9.6 PL DDR4 Memory

The PL side of the MPSoC is connected to 1 bank of DDR4-2400 SDRAM, 1GB x72, 8GB total + ECC

3.10 System Monitoring

The **9Z5** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using a TI MSP430 microcontroller (uC).

The microcontroller continually measures all voltage rails and temperature sensors and transmits the results to the FPGA, where they can be stored in blockram.

The following voltage rails and temperatures are monitored by the microcontroller:

| Monitor | Purpose |
|-------------|---|
| 12V0 | 12V Board Input Supply Voltage |
| 5V0 | 5V Board Input Supply Voltage |
| 3V3 | Board Input Supply Voltage |
| FMC_VADJ | Variable FMC IO Supply Voltage |
| 0V85 | FPGA Core Voltage |
| 1V8_DIG | FPGA PL side IO Supply Voltage |
| 1V8_PSAUX | FPGA PS Aux Supply Voltage |
| PS_AUXIO | FPGA PS Aux IO Supply Voltage |
| 1V8_PSAUX | FPGA PS Aux Supply Current |
| PS_AUXIO | FPGA PS Aux IO Supply Current |
| 1V8_DIG | FPGA PL side IO Supply Current |
| 12V0 | 12V Board Input Supply Current |
| Temp(1) | microcontroller internal temperature |
| Temp(4..2) | TMP422-EP internal temperatures (3 devices) |
| Temp(5) | FPGA on-die temperature (measured by TMP422-EP) |
| Temp(10..6) | pcb temperatures (5 different points - measured by TMP422-EP devices) |

Table 24 : Voltage and Temperature Monitors (in microcontroller)

3.10.1 Automatic Temperature Monitoring

The system monitor checks that the board and FPGA are being operated within the specified limits. If the temperature is close to the limit, a "Warning Alarm" interrupt is set.

If a limit is exceeded, a "Critical Alarm" interrupt is set. After the Critical Alarm is set, there is a 5 second delay before the system monitor unconfigures the FPGA by asserting its "PROG" pin.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

The temperature limits are shown in Table Temperature Limits. Note that the Min and Max values include a 5°C margin to prevent measurement errors triggering a false alarm.

| | Target FPGA | | | | Board (uC and PCB) | | | |
|------------|-------------|---------------|---------------|--------|--------------------|---------------|---------------|--------|
| | Min | Lower Warning | Upper Warning | Max | Min | Lower Warning | Upper Warning | Max |
| Extended | -5°C | +5°C | +95°C | +105°C | -5°C | +5°C | +80°C | +90°C |
| Industrial | -45°C | -35°C | +95°C | +105°C | -45°C | -35°C | +80°C | +90°C |
| Military | -60°C | -50°C | +140°C | +170°C | -60°C | -50°C | +125°C | +135°C |

Table 25 : Temperature Limits

3.10.2 System Monitor Status LEDs

LEDs D3 (Green) and D6 (Red) indicate the microcontroller status.

| LEDs | Status |
|---|--|
| Flashing Green + Flashing Red (alternate) | Service Mode |
| Red | Missing application firmware or invalid firmware |
| Red + Green | Standby (Powered off) |
| Green | Running and no alarms |
| Flashing Green + Red | Attention - alarm active |
| Flashing Green + Flashing Red (together) | Attention - critical alarm active |
| Flashing Red | FPGA configuration cleared to protect board |

Table 26 : System Monitor Status LEDs

3.11 FMC Interface and Front-Panel I/O

The FMC+ interface provides a high-performance and flexible front-panel interface through a range of interchangeable, industry standard IO modules which connect at receptacle J3.

The FMC+ interface adheres to VITA 57.4. The ADM-VPX3-9Z5 utilizes all possible FMC+ connectivity. This includes all GPIO, all MGT links, and all clock capable IO.

FMC I2C signal (SCL and SDA at C30 and C31) are connected to the system monitor microcontroller. They are used to determine operating voltage during startup and are not accessible to the user.

The FMC Present signal (PRSENT_M2C_L at connector pin H2) is connected to the system monitor microcontroller.

Note:

The ADM-VPX3-9Z5 supports only 1.8V and lower VADJ Voltages.

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Appendix A: P1 Pin Assignments

Appendix A.1: Data Plane 1 (P1 Wafers 1-4)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|----------|--------|------|--|------|--------|----------|
| P1_TX0_P | D1 | AY4 | | BA2 | A1 | P1_RX0_P |
| P1_TX0_N | E1 | AY3 | | BA1 | B1 | P1_RX0_N |
| P1_TX1_P | E2 | AW6 | | AW2 | B2 | P1_RX1_P |
| P1_TX1_N | F2 | AW5 | | AW1 | C2 | P1_RX1_N |

Table 27 : Data Plane 1 (P1 Wafers 1-4)

Appendix A.2: Data Plane 2 (P1 Wafers 5-8)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|----------|--------|------|--|------|--------|----------|
| P1_TX2_P | D3 | AU6 | | AV4 | A3 | P1_RX2_P |
| P1_TX2_N | E3 | AU5 | | AV3 | B3 | P1_RX2_N |
| P1_TX3_P | E4 | AT8 | | AU2 | B4 | P1_RX3_P |
| P1_TX3_N | F4 | AT7 | | AU1 | C4 | P1_RX3_N |

Table 28 : Data Plane 2 (P1 Wafers 5-8)

Appendix A.3: User Plane PS GTR(P1 Wafers 9-10)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|----------|--------|------|--|------|--------|----------|
| PS_TX2_P | D9 | AD39 | | AC41 | A9 | PS_RX2_P |
| PS_TX2_N | E9 | AD40 | | AC42 | B9 | PS_RX2_N |
| PS_TX3_P | E10 | AB39 | | AA41 | B10 | PS_RX3_P |
| PS_TX3_N | F10 | AB40 | | AA42 | C10 | PS_RX3_N |

Table 29 : User Plane PS GTR(P1 Wafers 9-10)

Appendix A.4: User Plane GPIO(P1 Wafers 11-12)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|------------|--------|------|--|------|--------|------------|
| GP9_1V8_P | A11 | AW11 | | AU11 | D11 | GP10_1V8_P |
| GP9_1V8_N | B11 | AW10 | | AV11 | E11 | GP10_1V8_N |
| GP11_1V8_P | B12 | AV12 | | BB5 | E12 | GP12_1V8_P |
| GP11_1V8_N | C12 | AW12 | | BB4 | F12 | GP12_1V8_N |

Table 30 : User Plane GPIO(P1 Wafers 11-12)

Appendix A.5: User Plane PS MIO(P1 Wafers 9-14)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|-----------|--------|------|--|------|--------|----------|
| PS_MIO_2 | D13 | T27 | | P27 | A13 | PS_MIO_0 |
| PS_MIO_3 | E13 | N30 | | N29 | B13 | PS_MIO_1 |
| PS_MIO_6 | E14 | R27 | | V29 | B14 | PS_MIO_4 |
| PS_MIO_7 | F14 | P29 | | W30 | C14 | PS_MIO_5 |
| PS_MIO_8 | G9 | P28 | | P30 | G11 | PS_MIO_9 |
| PS_MIO_10 | G13 | M28 | | - | - | - |

Table 31 : User Plane PS MIO(P1 Wafers 9-14)

Appendix A.6: Control Plane (P1 Wafers 15-16)

| Signal | VPX P1 | FPGA | | FPGA | VPX P1 | Signal |
|----------|--------|------|--|------|--------|----------|
| PS_TX1_P | D15 | AF39 | | AE41 | A15 | PS_RX1_P |
| PS_TX1_N | E15 | AF40 | | AE42 | B15 | PS_RX1_N |
| PS_TX0_P | E16 | AH39 | | AG41 | B16 | PS_RX0_P |
| PS_TX0_N | F16 | AH40 | | AG42 | C16 | PS_RX0_N |

Table 32 : Control Plane (P1 Wafers 15-16)

Appendix B: P2 Pin Assignments

Appendix B.1: GPIO (P2 Wafers 1-4)

| Signal | VPX P2 | FPGA | | FPGA | VPX P2 | Signal |
|--------|--------|------|--|------|--------|---------------|
| GP1_N | F4 | AK14 | | AN10 | E1 | GP7_N |
| GP1_P | E4 | AJ14 | | AM10 | D1 | GP7_P |
| GP2_N | C4 | AN13 | | AN11 | B1 | GP8_N |
| GP2_P | B4 | AM13 | | AM11 | A1 | GP8_P |
| GP3_N | E3 | AP14 | | B1 | G1 | GP_SE_3V3_<0> |
| GP3_P | D3 | AN14 | | C4 | G3 | GP_SE_3V3_<1> |
| GP4_N | B3 | AM14 | | C3 | G5 | GP_SE_3V3_<2> |
| GP4_P | A3 | AL14 | | C6 | G7 | GP_SE_3V3_<3> |
| GP5_N | F2 | AK15 | | C5 | G9 | GP_SE_3V3_<4> |
| GP5_P | E2 | AJ15 | | D2 | G11 | GP_SE_3V3_<5> |
| GP6_N | C2 | AM15 | | C1 | G13 | GP_SE_3V3_<6> |
| GP6_P | B2 | AL15 | | D4 | G15 | GP_SE_3V3_<7> |

Table 33 : GPIO (P2 Wafers 1-4)

Appendix B.2: MGT Pins (P2 Wafers 5-16)

| Signal | VPX P2 | FPGA | | FPGA | VPX P2 | Signal |
|----------|--------|------|--|------|--------|----------|
| P2_RX0_N | B5 | AM3 | | AL5 | E5 | P2_TX0_N |
| P2_RX0_P | A5 | AM4 | | AL6 | D5 | P2_TX0_P |
| P2_RX1_N | C6 | AL1 | | AK7 | F6 | P2_TX1_N |
| P2_RX1_P | B6 | AL2 | | AK8 | E6 | P2_TX1_P |
| P2_RX2_N | B7 | AK3 | | AJ5 | E7 | P2_TX2_N |
| P2_RX2_P | A7 | AK4 | | AJ6 | D7 | P2_TX2_P |
| P2_RX3_N | C8 | AJ1 | | AH7 | F8 | P2_TX3_N |
| P2_RX3_P | B8 | AJ2 | | AH8 | E8 | P2_TX3_P |
| P2_RX4_N | B9 | AH3 | | AG5 | E9 | P2_TX4_N |
| P2_RX4_P | A9 | AH4 | | AG6 | D9 | P2_TX4_P |
| P2_RX5_N | C10 | AG1 | | AF7 | F10 | P2_TX5_N |
| P2_RX5_P | B10 | AG2 | | AF8 | E10 | P2_TX5_P |
| P2_RX6_N | B11 | AF3 | | AE5 | E11 | P2_TX6_N |
| P2_RX6_P | A11 | AF4 | | AE6 | D11 | P2_TX6_P |

Table 34 : MGT (P2 Wafers 5-16) (continued on next page)

| Signal | VPX P2 | FPGA | | FPGA | VPX P2 | Signal |
|-----------|--------|------|--|------|--------|-----------|
| P2_RX7_N | C12 | AE1 | | AD7 | F12 | P2_TX7_N |
| P2_RX7_P | B12 | AE2 | | AD8 | E12 | P2_TX7_P |
| P2_RX8_N | B13 | AD3 | | AC5 | E13 | P2_TX8_N |
| P2_RX8_P | A13 | AD4 | | AC6 | D13 | P2_TX8_P |
| P2_RX9_N | C14 | AC1 | | AB7 | F14 | P2_TX9_N |
| P2_RX9_P | B14 | AC2 | | AB8 | E14 | P2_TX9_P |
| P2_RX10_N | C16 | AB3 | | AA5 | F16 | P2_TX10_N |
| P2_RX10_P | B16 | AB4 | | AA6 | E16 | P2_TX10_P |
| P2_RX11_N | B15 | AA1 | | Y7 | E15 | P2_TX11_N |
| P2_RX11_P | A15 | AA2 | | Y8 | D15 | P2_TX11_P |

Table 34 : MGT (P2 Wafers 5-16)

Appendix C: FMC Pin Assignments

Appendix C.1: GPIO Pins

| Signal | FMC (J3) | FPGA | FPGA | FPGA | FMC (J3) | Signal |
|-----------|----------|------|------|------|-----------|--------|
| LA00_CC_N | G7 | G20 | E14 | F5 | HA00_CC_N | |
| LA00_CC_P | G6 | H21 | F14 | F4 | HA00_CC_P | |
| LA01_CC_N | D9 | H19 | F15 | E3 | HA01_CC_N | |
| LA01_CC_P | D8 | H20 | G16 | E2 | HA01_CC_P | |
| LA02_N | H8 | E20 | N15 | K8 | HA02_N | |
| LA02_P | H7 | F20 | P15 | K7 | HA02_P | |
| LA03_N | G10 | E19 | L15 | J7 | HA03_N | |
| LA03_P | G9 | F19 | M15 | J6 | HA03_P | |
| LA04_N | H11 | J19 | K15 | F8 | HA04_N | |
| LA04_P | H10 | K19 | K16 | F7 | HA04_P | |
| LA05_N | D12 | K20 | G15 | E7 | HA05_N | |
| LA05_P | D11 | L20 | H15 | E6 | HA05_P | |
| LA06_N | C11 | L19 | M16 | K11 | HA06_N | |
| LA06_P | C10 | M20 | M17 | K10 | HA06_P | |
| LA07_N | H14 | B20 | N16 | J10 | HA07_N | |
| LA07_P | H13 | C20 | P16 | J9 | HA07_P | |
| LA08_N | G13 | C19 | K17 | F11 | HA08_N | |
| LA08_P | G12 | D19 | L17 | F10 | HA08_P | |
| LA09_N | D15 | J21 | A12 | E10 | HA09_N | |
| LA09_P | D14 | K21 | B13 | E9 | HA09_P | |
| LA10_N | C15 | J22 | D17 | K14 | HA10_N | |
| LA10_P | C14 | K22 | E17 | K13 | HA10_P | |
| LA11_N | H17 | D22 | H18 | J13 | HA11_N | |
| LA11_P | H16 | E22 | J18 | J12 | HA11_P | |
| LA12_N | G16 | B21 | F17 | F14 | HA12_N | |
| LA12_P | G15 | C21 | G17 | F13 | HA12_P | |
| LA13_N | D18 | A23 | H16 | E13 | HA13_N | |
| LA13_P | D17 | B23 | J16 | E12 | HA13_P | |
| LA14_N | C19 | D21 | C18 | J16 | HA14_N | |
| LA14_P | C18 | E21 | D18 | J15 | HA14_P | |
| LA15_N | H20 | A22 | C13 | F17 | HA15_N | |

Table 35 : GPIO Pins (continued on next page)

| Signal | FMC (J3) | FPGA | FPGA | FPGA | FMC (J3) | Signal |
|-----------|----------|------|------|------|-----------|--------|
| LA15_P | H19 | B22 | D13 | F16 | HA15_P | |
| LA16_N | G19 | A19 | F18 | E16 | HA16_N | |
| LA16_P | G18 | A20 | G18 | E15 | HA16_P | |
| LA17_CC_N | D21 | G27 | D14 | K17 | HA17_CC_N | |
| LA17_CC_P | D20 | G26 | E15 | K16 | HA17_CC_P | |
| LA18_CC_N | C23 | E25 | A17 | J19 | HA18_N | |
| LA18_CC_P | C22 | F25 | B17 | J18 | HA18_P | |
| LA19_N | H23 | N25 | A13 | F20 | HA19_N | |
| LA19_P | H22 | N24 | A14 | F19 | HA19_P | |
| LA20_N | G22 | N23 | D16 | E19 | HA20_N | |
| LA20_P | G21 | P23 | E16 | E18 | HA20_P | |
| LA21_N | H26 | A28 | A18 | K20 | HA21_N | |
| LA21_P | H25 | A27 | B18 | K19 | HA21_P | |
| LA22_N | G25 | L23 | B15 | J22 | HA22_N | |
| LA22_P | G24 | M23 | C15 | J21 | HA22_P | |
| LA23_N | D24 | L25 | B16 | K23 | HA23_N | |
| LA23_P | D23 | M25 | C16 | K22 | HA23_P | |
| LA24_N | H29 | G23 | C31 | K26 | HB00_CC_N | |
| LA24_P | H28 | H23 | C30 | K25 | HB00_CC_P | |
| LA25_N | G28 | B26 | F32 | J25 | HB01_N | |
| LA25_P | G27 | B25 | F31 | J24 | HB01_P | |
| LA26_N | D27 | K24 | H28 | F23 | HB02_N | |
| LA26_P | D26 | L24 | J28 | F22 | HB02_P | |
| LA27_N | C27 | J26 | A30 | E22 | HB03_N | |
| LA27_P | C26 | K26 | A29 | E21 | HB03_P | |
| LA28_N | H32 | E27 | H30 | F26 | HB04_N | |
| LA28_P | H31 | E26 | J30 | F25 | HB04_P | |
| LA29_N | G31 | F28 | F29 | E25 | HB05_N | |
| LA29_P | G30 | F27 | G28 | E24 | HB05_P | |
| LA30_N | H35 | D28 | D32 | K29 | HB06_CC_N | |
| LA30_P | H34 | D27 | E32 | K28 | HB06_CC_P | |
| LA31_N | G34 | B28 | F30 | J28 | HB07_N | |
| LA31_P | G33 | C28 | G30 | J27 | HB07_P | |
| LA32_N | H38 | J27 | D29 | F29 | HB08_N | |
| LA32_P | H37 | K27 | E29 | F28 | HB08_P | |
| LA33_N | G37 | B27 | C33 | E28 | HB09_N | |

Table 35 : GPIO Pins (continued on next page)

| Signal | FMC (J3) | FPGA | | FPGA | FMC (J3) | Signal |
|-------------|----------|------|--|------|----------|--------|
| LA33_P | G36 | C26 | | D33 | E27 | HB09_P |
| HB16_N | F35 | C37 | | A38 | K32 | HB10_N |
| HB16_P | F34 | C36 | | A37 | K31 | HB10_P |
| HB17_CC_N | K38 | B33 | | B30 | J31 | HB11_N |
| HB17_CC_P | K37 | B32 | | C29 | J30 | HB11_P |
| HB18_N | J37 | A34 | | A32 | F32 | HB12_N |
| HB18_P | J36 | A33 | | B31 | F31 | HB12_P |
| HB19_N | E34 | A40 | | A35 | E31 | HB13_N |
| HB19_P | E33 | A39 | | B35 | E30 | HB13_P |
| HB20_N | F38 | C34 | | B42 | K35 | HB14_N |
| HB20_P | F37 | D34 | | C42 | K34 | HB14_P |
| HB21_N | E37 | B37 | | B41 | J34 | HB15_N |
| HB21_P | E36 | B36 | | B40 | J33 | HB15_P |
| FMC_CLK_DIR | B1 | J17 | | - | - | - |

Table 35 : GPIO Pins

Appendix C.2: Clock Pins

| Signal | FMC (J3) | FPGA | | FPGA | FMC (J3) | Signal |
|---------------|----------|------|--|------|----------|---------------|
| CLK0_M2C_N | H5 | F22 | | H26 | K5 | CLK2_BIDIR_N |
| CLK0_M2C_P | H4 | F23 | | H25 | K4 | CLK2_BIDIR_P |
| CLK1_M2C_N | G3 | G21 | | G25 | J3 | CLK3_BIDIR_N |
| CLK1_M2C_P | G2 | G22 | | H24 | J2 | CLK3_BIDIR_P |
| GBTCLK0_M2C_N | D5 | AB35 | | L33 | L9 | GBTCLK3_M2C_N |
| GBTCLK0_M2C_P | D4 | AB34 | | L32 | L8 | GBTCLK3_M2C_P |
| GBTCLK1_M2C_N | B21 | W33 | | Y11 | L5 | GBTCLK4_M2C_N |
| GBTCLK1_M2C_P | B20 | W32 | | Y12 | L4 | GBTCLK4_M2C_P |
| GBTCLK2_M2C_N | L13 | R33 | | V11 | Z21 | GBTCLK5_M2C_N |
| GBTCLK2_M2C_P | L12 | R32 | | V12 | Z20 | GBTCLK5_M2C_P |

Table 36 : Clock Pins

Appendix C.3: MGT Pins

| Signal | FMC (J3) | FPGA | | FPGA | FMC (J3) | Signal |
|------------|----------|------|--|------|----------|------------|
| DP0_M2C_N | C7 | W42 | | Y35 | C3 | DP0_C2M_N |
| DP0_M2C_P | C6 | W41 | | Y34 | C2 | DP0_C2M_P |
| DP1_M2C_N | A3 | V40 | | W37 | A23 | DP1_C2M_N |
| DP1_M2C_P | A2 | V39 | | W36 | A22 | DP1_C2M_P |
| DP2_M2C_N | A7 | U42 | | V35 | A27 | DP2_C2M_N |
| DP2_M2C_P | A6 | U41 | | V34 | A26 | DP2_C2M_P |
| DP3_M2C_N | A11 | T40 | | U37 | A31 | DP3_C2M_N |
| DP3_M2C_P | A10 | T39 | | U36 | A30 | DP3_C2M_P |
| DP4_M2C_N | A15 | R42 | | T35 | A35 | DP4_C2M_N |
| DP4_M2C_P | A14 | R41 | | T34 | A34 | DP4_C2M_P |
| DP5_M2C_N | A19 | P40 | | R37 | A39 | DP5_C2M_N |
| DP5_M2C_P | A18 | P39 | | R36 | A38 | DP5_C2M_P |
| DP6_M2C_N | B17 | N42 | | P35 | B37 | DP6_C2M_N |
| DP6_M2C_P | B16 | N41 | | P34 | B36 | DP6_C2M_P |
| DP7_M2C_N | B13 | M40 | | N37 | B33 | DP7_C2M_N |
| DP7_M2C_P | B12 | M39 | | N36 | B32 | DP7_C2M_P |
| DP8_M2C_N | B9 | L42 | | M35 | B29 | DP8_C2M_N |
| DP8_M2C_P | B8 | L41 | | M34 | B28 | DP8_C2M_P |
| DP9_M2C_N | B5 | K40 | | L37 | B25 | DP9_C2M_N |
| DP9_M2C_P | B4 | K39 | | L36 | B24 | DP9_C2M_P |
| DP10_M2C_N | Y11 | J42 | | K35 | Z25 | DP10_C2M_N |
| DP10_M2C_P | Y10 | J41 | | K34 | Z24 | DP10_C2M_P |
| DP11_M2C_N | Z13 | H40 | | J37 | Y27 | DP11_C2M_N |
| DP11_M2C_P | Z12 | H39 | | J36 | Y26 | DP11_C2M_P |
| DP12_M2C_N | Y15 | G42 | | H35 | Z29 | DP12_C2M_N |
| DP12_M2C_P | Y14 | G41 | | H34 | Z28 | DP12_C2M_P |
| DP13_M2C_N | Z17 | F40 | | G37 | Y31 | DP13_C2M_N |
| DP13_M2C_P | Z16 | F39 | | G36 | Y30 | DP13_C2M_P |
| DP14_M2C_N | Y19 | E42 | | F35 | M19 | DP14_C2M_N |
| DP14_M2C_P | Y18 | E41 | | F34 | M18 | DP14_C2M_P |
| DP15_M2C_N | Y23 | D40 | | E37 | M23 | DP15_C2M_N |
| DP15_M2C_P | Y22 | D39 | | E36 | M22 | DP15_C2M_P |
| DP16_M2C_N | Z33 | Y3 | | W5 | M27 | DP16_C2M_N |
| DP16_M2C_P | Y35 | Y4 | | W6 | M31 | DP16_C2M_P |

Table 37 : MGT Pins (continued on next page)

| Signal | FMC (J3) | FPGA | | FPGA | FMC (J3) | Signal |
|------------|----------|------|--|------|----------|------------|
| DP17_M2C_N | Z37 | W1 | | V7 | M35 | DP17_C2M_N |
| DP17_M2C_P | Y39 | W2 | | V8 | M39 | DP17_C2M_P |
| DP18_M2C_N | M15 | V3 | | U5 | Z9 | DP18_C2M_N |
| DP18_M2C_P | M11 | V4 | | U6 | Y7 | DP18_C2M_P |
| DP19_M2C_N | M7 | U1 | | T7 | Z5 | DP19_C2M_N |
| DP19_M2C_P | M3 | U2 | | T8 | Y3 | DP19_C2M_P |
| DP20_M2C_N | Z32 | T3 | | R5 | M26 | DP20_C2M_N |
| DP20_M2C_P | Y34 | T4 | | R6 | M30 | DP20_C2M_P |
| DP21_M2C_N | Z36 | R1 | | P7 | M34 | DP21_C2M_N |
| DP21_M2C_P | Y38 | R2 | | P8 | M38 | DP21_C2M_P |
| DP22_M2C_N | M14 | P3 | | N5 | Z8 | DP22_C2M_N |
| DP22_M2C_P | M10 | P4 | | N6 | Y6 | DP22_C2M_P |
| DP23_M2C_N | M6 | N1 | | M7 | Z4 | DP23_C2M_N |
| DP23_M2C_P | M2 | N2 | | M8 | Y2 | DP23_C2M_P |

Table 37 : MGT Pins

Revision History

| Date | Revision | Nature of Change |
|--------------|----------|------------------------|
| 13 May 2020 | 0.1 | Initial Draft |
| 27 July 2020 | 0.2 | Updated images |
| 08 June 2021 | 1.0 | Production Release |
| 10 Nov 2021 | 1.1 | Updated FMC GPIO table |